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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/647,468	08/26/2003	Osamu Abe	2002-249352US	2305
21254 7	590 02/09/2005	EXAMINER		INER
MCGINN & GIBB, PLLC 8321 OLD COURTHOUSE ROAD			ENGLUND, 1	TERRY LEE
SUITE 200	OKTHOOSE KOMD		ART UNIT	PAPER NUMBER
VIENNA, VA 22182-3817			2816	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

An

		Application No.	Applicant(s)				
Office Action Summary		10/647,468	ABE, OSAMU				
		Examiner	Art Unit				
		Terry L. Englund	2816				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1)⊠ Responsive to	communication(s) filed on 08 Oc	ctober 2005 and 18 November 20	<u>004</u> .				
3)☐ Since this app	· ·						
closed in acco	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
4)⊠ Claim(s) <i>1-22</i>	is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.							
5)☐ Claim(s)							
6)⊠ Claim(s) <u>1-3,5</u>	5,6,8-10,13,14,16,17,20 and 22 is	/are rejected.					
7)⊠ Claim(s) <u>4,7,1</u>	1,12,15,18,19 and 21 is/are object	cted to.					
8) Claim(s)	_ are subject to restriction and/or	election requirement.					
Application Papers	Application Papers						
9)☐ The specification	on is objected to by the Examiner						
			ed to by the Examiner.				
10)☑ The drawing(s) filed on <u>18 November 2004</u> is/are: a)☑ accepted or b)回 objected to by the Examiner.  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C	C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) △ All b) □ Some * c) □ None of:							
1.⊠ Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents have been received in Application No							
3. Copies of the certified copies of the priority documents have been received in this National Stage							
application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list of the certified copies not received.							
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 4) Interview Summary (PTO-413) Paper No(s)/Mail Date							
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 5) Notice of Informal Patent Application (PTO-152)							
Paper No(s)/Mail Date <u>10082004</u> . 6)							

#### **DETAILED ACTION**

#### Response to Amendment/Translation

The amendment, translation, and drawings submitted on Nov 18, 2004 were reviewed and considered with the following results.

The certified English translation of the priority document overcame all of the prior art rejections described in the previous Office Action. Therefore, the following rejections have been withdrawn: 1) claim 1 under 35 U.S.C. 102(e) with respect to Mottola et al.; and 2) claims 2-3, and 5-6 under 35 U.S.C. 103(a) with respect to Mottola et al./Oda. The Mottola et al. reference was filed on Sep 3, 2002, wherein the priority document has a date of Aug 28, 2002.

However, after reconsidering the claims, including newly added claims 8-22, it was noted other prior art references read on the broadest reasonable interpretation of at least some of the recited limitations. Therefore, new rejections are described later under the appropriate section. Since only rejections under 35 U.S.C. 102(e) had been cited previously, this action in NON-FINAL.

The replacement sheets of drawings have been approved, and the drawing objections described in the previous Office Action have now been withdrawn. However, it is noted that although the objections to the use of P01, P02, N01, and C01 had not been addressed, the action's objection had inadvertently identified them with Fig. 1, wherein they are actually shown in PRIOR ART Fig. 8. These components are understood to form one type of start up circuitry, and since they are only shown in the PRIOR ART figure, those objections have been withdrawn.

The new abstract, and the amended sections of the specification, overcame all of their respective objections described in the previous Office Action. Although those objections have

been withdrawn, it is not understood where the "paragraph commencing at page 3, line 24" is amended (i.e. see page 2 of the amendment). Therefore, that paragraph is now objected to, as described later under the appropriate section.

### Specification

The amended "paragraph commencing at page 3, line 24" on page 2 of the amendment is objected to because of the following informalities: Since the amended change is not clearly shown, it is suggested that paragraph be re-submitted with the intended change identified. Also, it is suggested the phrase --gate of-- be added after "has the" on line 4 of the paragraph to more clearly identify what is actually connected between P2 and N2. An appropriate correction is required.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 10, and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by McNeill et al. (McNeill), a reference cited as being of special interest on page 9 of the previous Office Action. However, that action had not used the reference in any prior art rejections. Fig. 1 shows a band gap circuit generating output voltage VREG at circuit output terminal 126, wherein the circuit is connected to power supply voltage source VDD and reference potential point VSS. The circuit comprises differential amplifier 112 having inverting input terminal – (receiving a potential from node N2), noninverting input terminal + (receiving a potential from node N1), and

an output terminal (providing potential VGATE; one of ordinary skill in the art would understand first circuit 160,R1,Q1-Q2 causes a potential difference to occur at the input terminals in response to fluctuation of voltage VREG; and switching element M3 causes excess current from circuit output terminal 126 to flow to reference potential GND (via M4) in response to output potential VGATE of differential amplifier 112. For example, any current flowing through M3 can be considered an excess current with respect to the current flowing through the current paths that include transistors M1 and M2. Since switching element M3 is connected to circuit output terminal 126, reference potential point VSS (via M4), and directly to the output terminal of differential amplifier 112, claim 1 is anticipated. Deeming 150 as one type of a voltage supply (e.g. a voltage drop) circuit connected to power supply voltage source VDD, claim 10 is also anticipated. Fig. 5B shows first element M11, with resistive component M11 (i.e. the control electrode of PMOS transistor M11 is coupled to ground, and therefore the transistor will function as a resistive component), and second element CF, with capacitive component CF. McNeill discloses the Fig. 5B configuration improves power supply rejection ratio (PSRR), which one of ordinary skill in the art can relate to removing power supply noise. Therefore, when differential amplifier 112 also includes Fig. 5B, claims 2-3 and 13-14 are also anticipated.

Claims 1, and 10 are also rejected under 35 U.S.C. 102(b) as being anticipated by Tokuda, a reference found during an update search. Fig. 1 shows a band gap type circuit for generating output voltage Vout from circuit output terminal Tout, wherein the band gap type circuit is connected to power supply voltage source Vcc and reference potential point GND. The circuit comprises differential amplifier 14 having inverting input terminal – (receiving potential

Vref), noninverting input terminal + (receiving potential Vs), and an output terminal (providing potential (Vs-Vref); first circuit 12,13 causes a potential difference to occur at the input terminals in response to fluctuation of voltage Vout (e.g. see column 1, lines 15-25 and 36-50); and switching element Q11 causes excess current from circuit output terminal Tout to flow to reference potential GND in response to the output potential (Vs-Vref) of differential amplifier (i.e. see columns 1 (lines 23-25 and 57-60) and 2 (lines 4-12 and 48-51)). Since switching element Q11 is connected to circuit output terminal Tout, reference potential point GND, and directly to the output terminal of differential amplifier 14, claim 1 is anticipated. Deeming R11 as one type of a voltage supply (e.g. a voltage drop) circuit connected to power supply voltage source Vcc, claim 10 is anticipated.

#### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3, and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokuda as applied to claims 1 and 10 above, respectively and further in view of Oda, a reference cited in the previous Office Action. Although the reference of Tokuda reads on the basic differential amplifier/first circuit/switching element limitations recited within independent claims 1 and 10, the reference does not clearly show or disclose first/second elements for removing power supply noise, the first element comprising a transistor, or the switching element as an N-channel MOS transistor. Fig. 1 of Oda shows a low pass filter (LPF) R1,C1,C2 coupled to output

A of reference voltage generating source 1, wherein the LPF removes noise from the power source (e.g. see column 1, lies 29-33). Therefore, it would have been obvious to one of ordinary skill in the art to apply a filter, such as shown by Oda's Fig. 1, to output terminal Tout of Tokuda. For example, first element R1,C1 could be coupled between Tokuda's power supply voltage Vcc and output terminal Tout, and second element C2 could be coupled between output terminal Tout and reference potential point GND. Since first element R1,C1 has resistive component R1, and second element C2 has capacitive component C2, claims 2 and 13 are rendered obvious. This filter would remove power supply noise, and one of ordinary skill in the art would understand the specific size and type of filter (components) would depend on the overall circuit's environment, and type of noise to be removed. It also would have been obvious to one of ordinary skill in the art to replace resistive component R1 with a transistor, thus rendering claims 3 and 14 obvious. A transistor would provide one means for adjusting or tuning the filter characteristics to achieve the desired results by varying the bias voltage applied to the control electrode of the transistor, thus tuning the filter by varying the resistance of the transistor would be possible, if required.

Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokuda as applied to their respective independent claim 1 or 10 described above. Although the reference of Tokuda reads on the basic differential amplifier/first circuit/switching element limitations recited within independent claims 1 and 10, the reference shows switching element Q11 as an NPN bipolar transistor instead of an N-channel MOS transistor. It would have been obvious to one of ordinary skill in the art to replace NPN transistor Q11 with an N-channel MOS transistor in Tokuda's circuit to function as a switch, rendering claims 8 and 16 obvious. The N-channel

MOS transistor is functionally equivalent to an NPN transistor as one type of switching element, and is easier to fabricate and utilizes less energy (e.g. lower voltages) than a bipolar transistor, if that would be desired within the overall circuit.

Claims 5-6, 9, 17, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokuda/Oda for the same reasons as applied to corresponding claims 2-3, 8, 13-14, and 16 previously described above. For example, it would have been obvious to one of ordinary skill in the art to combine voltage supply circuit R11, differential amplifier 14, first circuit 12,13, and switching element Q11 of Tokuda's Fig. 1 with the use (e.g. teachings) of Oda's filter (e.g. first/second elements R1,C1/C2, wherein first element R1,C1 has resistive component R1, and second element C2 has capacitive component). Also, as previously described, first element component R1 could be a transistor for adjusting the filter characteristics; and switching element Q11 could be an N-channel MOS transistor. Therefore, claims 5-6, 9, 17, 20, and 22 are rendered obvious for the same reasons as applied to the other, previously rejected claims.

No claim is allowable as presently written.

### Allowable Subject Matter

However, claims 4, 7, 11-12, 15, 18-19, and 21 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the second element comprises an ion implantation resistor as recited within claims 4, 7, 15, and 21; or 2) the voltage supply circuit comprises the constant current source and transistors as recited within claims 11-12, and 18-19.

Application/Control Number: 10/647,468

Art Unit: 2816

Prior Art

Page 8

The prior art references cited on the IDS submitted Oct 8, 2004 were reviewed and

considered. None of these references clearly shows or discloses the switching element for

causing excess current from the output terminal to flow to the reference potential as recited

within each of independent claims 1, 10, and 17.

Any inquiry concerning this communication from the examiner should be directed to

Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be

reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent

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system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry L. Englund

1 February 2005

TIMOTHY P. CALLAHAN

UP ERVISORY PATENT EXAMINER

**TECHNOLOGY CENTER 2800**